**1. DRC energy, attack, deday time constant registers ae, aa, ad**

**(Address DRC1: 0X3A, 0X3B, 0x3C; DRC2: 0X3D, 0x3E and 0x3F)**

All the time constants are in Q3.23 format.

The relationship between the time constant t and the register is defined as below



example:

fs = 48KHz,

when DRC 1, energy time constant ta = 1s, attack time = 100ms, delay time = 500ms

ae = 1 - e^(-1/fs/te) = 2.0833116\*e-5 = 0x0000 00AF in Q3.23

aa = 1 - e^(-1/fs/ta) = 2.0831163\*e-4 = 0x0000 06D3 in Q3.23

ad = 1 - e^(-1/fs/td) = 4.1665799\*e-5 = 0x0000 015E in Q3.23

we = 1-ae = 0x007F FF51

wa = 1-aa = 0x007F F92D

wd = 1-ad = 0x007F FEA2

Then

0x3A = 0x0000 00AF 007F FF51

0x3B = 0x0000 06D3 007F F92D

0x3C = 0x0000 015E 0x007F FEA2

**2. DRC threshold T (Addressx040, 0x43)**

The threshold T is in Q9.23 format.

The relationship between the DRC threshold value TdB and the register value T is :

T = (TdB-24)/-6.0206

*Example:*

when DRC1 TdB = -64dB, T = (-64-24)/-6.0206 = 14.62 = 0 0000 1110. 1101 1101 0001 1101 101 = 0x074E E8ED in Q9.23

then 0x40 = 0x074E E8ED

**3. DRC slope parameter K (0x41, 0x44)**

K is in Q3.23 format

In developing the equations used to determine the K value required to realize a given compression or expansion within a given region of the DRC, the following convention has been adopted.

DRC Transfer = Input Increase: Output Increase

If the DRC realizes an output increase of n dB for every dB increase in the RMS value of the audio into the DRC, a 1:n expansion is being performed. If the DRC realizes a 1-dB increase in output level for every n dB increase in the RMS value of the audio into the DRC, an n:1 compression is being performed.

For a 1:n expansion, the slope k can be found by : K = n – 1

For an n:1 compression, the slope k can be found by: K = 1/N - 1

*Example:*

1).



when the DRC1 input increase 1dB, the output increase 3dB, it's a 1:3 expansion, n = 3 and then k = 3-1 = 2 in Q3.23

0x41 = 0x0100 0000

2).



When the input increase 1dB, the output increase 0.5dB, it's a 2:1 compression, n = 2 and then K = 1/2-1 = -0.5 in Q3.23

0x41 = 0x03C0 0000

**4 DRC offset O (0x42, 0x45)**

O is in Q9.17 format

The relationship between the DRC offset value Ggd and the register value Goffset is defined as:

Goffset = 10^(Ggd/20)/15.5;

example:

when DRC 1 offset = +6 dB

Goffset = 10^(6/20)/15.5 = 0.13170048 = 0x0010 DB90 in Q3.23

0x42 = 0x0010 DB90

**DRC 输入/输出 GUI**



offset让用户在offset框中输入值

DRC输入/输出关系界面让用户配两个点threshold和max output, threshold可以左右拖动，max output 可以上下拖动。 图形确定以后根据**2. DRC threshold T (Addressx040, 0x43)**

计算T寄存器的值， 根据**3. DRC slope parameter K (0x41, 0x44)** 计算K寄存器的值

**DRC 寄存器参数范围**

|  |  |  |
| --- | --- | --- |
| **Name** | **Range** | |
| **Min** | **Max** |
| **Energy/Attack/Decay Time** | **0s** | **20s** |
| **Threshold** | **-120dB** | **+24dB** |
| **Slope** | **-3** | **+5-2-23** |
| **Offset** | **0** | **+35.8dB** |

**DRC 内部参数范围**

|  |  |  |
| --- | --- | --- |
| **Name** | **Range** | |
| **Min** | **Max** |
| **Output** | **-144dB** | **+24dB** |
| **Gain** | **0** | **+36dB** |